

ABSTRACT OF THE DISCLOSURE

A floating point total order comparator circuit for comparing a first floating point operand and a second floating point operand includes a first analysis circuit for determining a format of the first floating point operand based upon floating point status information encoded within the first floating point operand, a second analysis circuit for determining a format of the second floating point operand based upon floating point status information encoded within the second floating point operand, and a result generator circuit coupled to the analysis circuits for producing a result indicating a total order comparative relationship between the first floating point operand and the second floating point operand based on the format of the first floating point operand and the format of the second floating point operand. The result can condition the outcome of a floating point instruction. The floating point total order comparator circuit may recognize several predetermined operand formats, such as not-a-number (NaN), infinity, normalized, denormalized, invalid operation, overflow, underflow, division by zero, positive zero, negative zero, exact, and inexact.